24 Bit Digital Accelerometers

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INTRODUCTION

Rapid advances in high quality sensors and integrated circuits have enabled the affordable realization of very high resolution digital output devices. New analog to digital converters and piezoelectric accelerometers are being combined to deliver unprecedented broadband resolution and noise immunity. Standardization of the interface between digital sensors and microcontrollers provides for cost effective measurement system development. Applications such as condition-based maintenance and structural acoustics are poised to expand rapidly with the advent of this technology.

APPLICATIONS

Condition-based maintenance of machinery and structural acoustics monitoring and control demand exceptional performance from vibration sensing systems. In order to effectively diagnose incipient bearing or gear faults, it is not unusual that a vibration sensor must resolve micro-G's in the presence of tens of G's of vibration.[1] In structural acoustics, the fidelity and response of the human ear is keenly sensitive to the limitations of a vibration sensor. The ability to monitor and control noise producing structural vibration pits the capability of an accelerometer directly with that of the human ear.

PIEZO-SENSORS

Piezoelectric accelerometers are nearly ideal complements for the bandwidth and dynamic range requirements of these applications. The piezoelectric transduction element is capable of delivering more than 180 dB dynamic range over frequency ranges in excess of 20 kHz.

The resolution of a spring/mass piezo-transduction element is fundamentally limited by thermal or Brownian noise. The fluctuation dissipation theorem assures that the Nyquist force responsible for the Brownian motion of a spring mass system is given by the following expression, written in terms of the acceleration of the proof mass;

$$a_{Brownian} = \left(\frac{4kT\omega_o}{mQ} \right)^{1/2} \frac{m}{\sec^2} \frac{1}{\sqrt{Hz}}$$

where k is Boltzmann's constant, $k=1.38 \times 10^{-23}$ Joule/°K, T is the temperature in °K, ω_o is $\sqrt{k_s/m}$, k_s is the equivalent spring stiffness of the piezo-material, m is the proof mass and Q is the mechanical quality factor (an expression for damping).

For a modest, low cost, miniature accelerometer; m=1gram, ω_o= (2Π)(40kHz) rad/sec and Q=1000. k_s is calculated to be 63 x 10^6 kg/m. The fundamental resolution limit $a_{Brownian}$ is the calculated to be approximately 4 x 10^{-15} m/sec^2 or about 0.4 femto G's.

It seems apparent that the resolution of a typical piezo-accelerometer is probably defined by the electrical noise or accompanying electronics (see next section.) Thermal noise due to electrical and mechanical losses can be derived as;[2]

$$a_{thermal} = \left(\frac{4kT \tan \delta}{\omega M^2 C} \right)^{1/2} \frac{m}{\sec^2} \frac{1}{\sqrt{Hz}}$$

where tan δ is the piezo-material's dielectric dissipation factor, ω is frequency, M is sensitivity of accelerometer in m/sec^2 and C is capacitance of the piezo-material. Working with the same typical accelerometer above where tan δ is 2, ω = (2Π)(10 Hz), M = 0.001 V/(m/sec^2) and C = 100 x 10^{-12} Farads; the resolution at 10 Hz is estimated at 5 x 10^{-6} m/sec^2 or about 0.5 microG's.

Elastic deformation of piezo-material establishes the full scale output of the transduction element. Although published material properties of piezo-ceramics are scarce to come by, experience shows that the example sensor discussed above remains in its elastic region for at least 2000 G's of excitation (shock survivability is ten times higher.) Considering the theoretical resolution limit of thermal noise and the linear full scale amplitude output established above, the dynamic range of the piezo-ceramic accelerometer at 10 Hz is estimated at 10^9 or 180 dB!

FET PREAMPLIFIERS

The signal generated from a piezoelectric material source requires a preamplifier to deliver full frequency response and noise immunity to any electronics measurement system. Analog FET preamplifiers are utilized to condition this characteristic high impedance signal prior to filtering and digitizing. These transistor circuits usually establish the dynamic range of the sensor. Intrinsic transistor noise, thermal resistor noise and the supply voltage are typically the boundaries of this limitation.

The voltage noise limit of an inverting preamplifier (or charge amplifier), expressed in terms of acceleration, is given by;[2]

$$a_{resolution} = \left[a_{thermal}^2 + \frac{1}{M^2} \left(\frac{C + C_i + C_f}{C} \right)^2 \left(1 + \left(\frac{\omega_o}{\omega} \right)^\alpha \right) e_o^2 + \frac{1}{M^2} \frac{1}{(\omega C)^2} \left(\frac{4kT}{R_f} + i_A^2 \right) \right]^{1/2} \frac{m}{\sec^2} \frac{1}{\sqrt{Hz}}$$

where C_i is amplifier plus cable capacitance at input; C_f is amplifier feedback capacitance; ω_o, e_o, α and i_A are FET amplifier internal noise properties; and R_f is amplifier feedback resistance. A good JFET Op Amp (such as the TI TLC2201) has an intrinsic noise contribution of about 20 nanoV/$\sqrt{Hz}$ at 10 Hz. With ±5 V range, the preamplifier alone typically reduces the useable dynamic range of the sensor signal to about 160 dB. The addition of other noise sources such as power supply noise reduces the dynamic range of the piezo-transduction element and preamplifier to something on the order of 120 dB.

SIGMA-DELTA ADC's

The advent of low cost, high quality sigma-delta analog to digital converters (ADC's) has enabled the development of a new generation of sensors capable of being interfaced directly with microprocessors and microcontrollers. The sigma-delta architecture provides for exceptionally cost effective transformation of high dynamic range analog signals to the digital domain.[3]

The number of bits in an ADC can be misleading. As trends continue toward a combination of more sample resolution and bandwidth, static measures of performance like non-linearity are giving way to dynamic measures such as signal-to-noise ratio and distortion dynamic range. A case in point is the sigma-delta converter which may use a single-bit converter yet achieve over 20 effective bits of dynamic range.

The sigma-delta conversion architecture typically uses a 1-bit analog-to-digital converter operating at a very high rate which redistributes quantization noise to beyond the frequency band of interest. The total noise energy remains constant, but by spreading it over a much wider spectrum, the amount of noise in the frequency band of interest is reduced. The architecture of the sigma-delta is usually separated by analog modulation and digital decimation. Noise shaping is performed in the modulator usually with switched-capacitors, and the oversampled signal is given to the decimator. There the signal goes through filtering, quantization noise removal, and decimation.

Dithering is a method for randomizing the quantization errors of an ADC by adding a stimulus which is uncorrelated to the signal at the ADC input. Various types of dithering can be characterized by the basis of noise, amplitude (small scale or large scale), or frequency (narrow or broadband). Improvements in the converters performance varies with the degree and type of dithering and filtering used, but typically can extract signals below the ADC's least significant bit (LSB). These recent advances have pushed converter technology to reach sample rates of over 25 MSPS while achieving up to 23 bits of effective resolution, which correspond to signals of -140 dBm. [4]

Audio markets have driven development of this technology to the point that it is practical to produce pass bands as high as 48 kHz with 24 bit resolution. Trends have been toward single-supply, high bandwidth, 5th/7th order modulators, integrated references, on-board controllers, and anti-aliasing filters. Recent commercial chips have surfaced; designed specifically with operating Vdd of 2.7V and lower for battery powered operation.

Particular technical challenges to note with these systems are high 1/f noise and filter settling time. Achieving 24 bit resolution is hardly as trivial as selecting an ADC and prototyping a system. Distortion and digital noise feedthrough are significant design challenges when dealing with this type of resolution. Board layout with high resolution converters requires careful attention. Trace impedance, ground drops, inductive and capacitive coupling, and separation of analog from digital signals, need to be considered. Isolation and shielding are paramount to preserving the precious 120 dB dynamic range at the output of a piezo-sensor's preamp stage.

NETWORKING

Standards for interfacing ADC's to microprocessors has long been a challenge to industry. The first solutions were parallel interfaces that required as many interconnects as bits delivering full frequency bandwidth digital data in real time. The need to reduce cost and improve reliability drove the implementation of serial interfaces. Popular standards in use today are SPI or I2C. Nearly every manufacturer of microprocessors and microcontrollers has a version of this to suit integrated design needs. As few as three wires are used to communicate and regulate data interchange. For "deterministic" sensor measurement systems (where all relevant sensor information is known for each channel), this is a powerfully simple system architecture.

One of the most important advantages of the sensor's digital output, is the flexibility of manipulating the information in the digital domain. Advantages include networking a digital

sensor to plug and play on a digital bus, uploading sensor personalities when a new device is installed on the network, greater noise immunity during transmission, and using error checking, fault tolerance and digital compensation to add robustness. Generally, converter sampling (start conversion) and converter output can be synchronous or asynchronous depending on the system requirements. The system tradeoff is bandwidth versus simultaneous sampling over networked devices. Handshaking protocol requirements present some overhead and ultimately slow the converters throughput.

Arrays of sensors need to synchronize their conversions to preserve important information relative to the array. Some examples of this array information can be displacement, vector location, relative position, or phase. In order to maintain phase matching to within 1 degree over 20 kHz, synchronization within roughly 1 nanosecond is required. This presents quite a challenge for distributed timing devices. Without guaranteed access to the high frequency GPS clock, fiber optic time synchronizing is necessary to meet high phase accuracy and bandwidth over distance in an array.

There is a new interface standard afoot that aims to make digital sensors interoperable between any microprocessor based system. The IEEE has been hard at work on P1451 defining the issues and developing a standard that would allow all the "deterministic" measurement information about a transducer to be stored internally and communicated over a network interface. The second part of this proposed standard identifies the interface between digital transducers and microprocessors. The current proposal indicates the need for as many as 10 interconnects in order to be able to effectively pass data and transducer data sheet information without compromise. Clearly there is a need to balance the needs of performance with that of reliability. Major suppliers such as Analog Devices have taken a lead role in developing these standards. Time will tell exactly what is the right balance.

CONCLUSION

The practicality of the digital output sensor is revamping the architecture of measurement systems. Measurement accuracy will be the net benefit with improved fidelity and noise immunity. The natural progression of this technology is leading to eventual realization of intelligent transducer arrays. Time synchronization and network communication bandwidth remain technical challenges on the path to this realization.

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